

699 HF  
Appl. No. 10/669,012

Amdt. dated April 6, 2006

Reply to Office Action of December 8, 2005

PATENT

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1. (Currently Amended) An integrated circuit comprising:  
partially reconfigurable programmable circuit elements for alternately implementing a first circuit and a second circuit; and  
a finite state machine,  
wherein the finite state machine configures the partially reconfigurable programmable circuit elements to implement the first circuit to detect boundaries between words in an input data stream,  
when the finite state machine determines when the partially reconfigurable programmable circuit elements correctly indicate boundaries between frames in the input data stream, and the finite state machine reconfigures overwrites at least a portion of the first circuit partially reconfigurable programmable circuit elements to implement the second circuit to align the words in the input data stream based on the detected word boundaries and to determine when the word boundaries have changed, and  
when the finite state machine determines the word boundaries have changed, the finite state machine overwrites at least a portion of the second circuit to implement the first circuit to detect boundaries between words in the input data stream.
2. (Original) The integrated circuit according to claim 1 further comprising:  
data and overhead processing circuitry.
3. (Original) The integrated circuit according to claim 1 further comprising:  
input/output circuitry that receives the input data stream.
4. (Original) The integrated circuit according to claim 1 wherein the integrated circuit includes portions of hardwired, application-specific circuitry.

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5. (Original) The integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array.
6. (Original) The integrated circuit according to claim 1 wherein:  
the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate framing patterns in SONET input data.
7. (Original) The integrated circuit according to claim 6 wherein:  
the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align frames in the SONET input data stream based on the detected boundaries.
8. (Original) The integrated circuit according to claim 1 wherein:  
the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate framing patterns in SDH frames in the input data stream.
9. (Original) The integrated circuit according to claim 8 wherein:  
the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align frames in the SDH input data based on the detected boundaries.
10. (Original) The integrated circuit according to claim 1 wherein:  
the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate training patterns in OIF SPI4 phase 2 input data.
11. (Original) The integrated circuit according to claim 10 wherein:  
the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align channels in the OIF SPI4 phase 2 input data based on the detected training patterns.
12. (Currently Amended) A method comprising:  
configuring reconfigurable programmable circuit elements to implement a first circuit to detect boundaries between words in input data using a finite state machine, wherein the

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finite state machine determines when the reconfigurable programmable circuit elements correctly indicate boundaries between frames in the input data; and

overwriting at least a portion of reconfiguring the first circuit reconfigurable programmable circuit elements to implement a second circuit to align the words in the input data based on the detected word boundaries and to determine when the word boundaries have changed using the finite state machine, and

overwriting at least a portion of the second circuit when the finite state machine determines the word boundaries have changed in order to implement the first circuit to detect boundaries between words in input data using a finite state machine.

13. (Original) The method of claim 12 further comprising:  
processing overhead and data bytes in the input data using data and overhead processing circuitry.

14. (Original) The method of claim 12 further comprising:  
receiving the input data at input/output circuitry.

15. (Currently Amended) The method of claim 12 wherein the method is implemented using an integrated circuit includes including portions of hardwired, application-specific circuitry.

16. (Currently Amended) The method of claim 12 wherein the method is implemented using an integrated circuit that is a field programmable gate array, and the reconfigurable programmable circuit elements are partially reconfigurable.

17. (Original) The method of claim 12 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:  
reconfiguring the partially reconfigurable programmable circuit elements to locate framing patterns in SONET input data using the finite state machine.

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18. (Original) The method of claim 17 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:  
reconfiguring the partially reconfigurable programmable circuit elements to align frames in the SONET input data stream based on the detected boundaries.

19. (Original) The method of claim 12 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:  
reconfiguring the partially reconfigurable programmable circuit elements to locate framing patterns in SDH input data using the finite state machine.

20. (Original) The method of claim 19 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:  
reconfiguring the partially reconfigurable programmable circuit elements to align frames in the SDH input data based on the detected boundaries.

21. (Original) The method of claim 12 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:  
reconfiguring the partially reconfigurable programmable circuit elements to locate training patterns in OIF SPI4 phase 2 input data.

22. (Original) The method of claim 20 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:  
reconfiguring the partially reconfigurable programmable circuit elements to align channels in the OIF SPI4 phase 2 input data based on the detected training patterns.